IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS

FLASH-CONTROL, LLC Plaintiff, v. MICRON TECHNOLOGY, INC. Defendant.	**Civil Action No. 6:20-cv-361** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Flash-Control, LLC ("Flash-Control" or "Plaintiff"), for its Complaint against Defendant Micron Technology, Inc., (referred to herein as "Micron" or "Defendant"), alleges the following:

NATURE OF THE ACTION

1. This is an action for patent infringement arising under the Patent Laws of the United States, 35 U.S.C. § 1 *et seq*.

THE PARTIES

2. Plaintiff Flash-Control is a limited liability company organized under the laws of the State of Delaware, and its registered agent for service of process in Delaware is Rita Carnavale, 717 North Union Street, Wilmington, Delaware, 19805.

3. Upon information and belief, Micron is a corporation organized under the laws of the Delaware with a place of business at 8000 South Federal Way PO Box 6, Boise, ID 83716, and with offices at 101 W Louis Hanna Blvd., Austin, TX 78728. Upon information and belief, Micron sells, offers to sell, and/or uses products and services throughout the United States, including in this judicial district, and introduces infringing products and services into the stream

of commerce knowing that they would be sold and/or used in this judicial district and elsewhere in the United States.

JURISDICTION AND VENUE

4. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code.

5. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

6. Venue is proper in this judicial district under 28 U.S.C. § 1400(b).

7. This Court has personal jurisdiction over Micron under the laws of the Texas, due at least to their substantial business in Texas and in this judicial district, directly or through intermediaries, including: (i) at least a portion of the infringements alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent courses of conduct and/or deriving substantial revenue from goods and services provided to individuals in the State of Texas. Venue is also proper in this district because Micron has a regular and established place of business in this district. For instance, Micron has a research, development, and corporate offices in this judicial district. For example, Micron has a research, development, and corporate office located at 101 W Louis Hanna Blvd., Austin, TX, 78728. (*See, e.g.*, https://www.google.com/search?rlz=1C5CHFA_enUS826US826&ei=H5KDXsm5DIj4tAWyr52QAQ&q=Austin%2C+TX%2C+78728+micron&oq=Austin%2C+TX%2C+78728+micron&gs_lcp=CgZwc3ktYWIQA1DP4AJYz-ACYOfiAmgAcAB4AIABc4gByAGSAQMxLjGYAQCgAQGqAQdnd3Mtd2l6&sclient=psy-ab&ved=0ahUKEwiJxZLjscXoAhUIPK0KHbJXBxIQ4dUDCAs&uact=5.)

BACKGROUND

The Invention

8. Mohan Rao is the inventor of U.S. Patent Nos. 9,257,184 ("the '184 patent"), 9,792,219 ("the '219 patent"), 8,531,880 ("the '880 patent"), and 8,817,537 ("the '537 patent"). A true and correct copy of the '184 patent is attached as Exhibit A. A true and correct copy of the '219 patent is attached as Exhibit B. A true and correct copy of the '880 patent is attached as Exhibit C. A true and correct copy of '537 is attached as Exhibit D.

9. The '184, '219, '880, and '537 patents resulted from the pioneering efforts of Dr. Rao (hereinafter "the Inventor") in the area of nonvolatile memory systems. These efforts resulted in development and patent applications entitled "NONVOLATILE MEMORYSYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES" with development starting in the early 1990s. At the time of these pioneering efforts, the most widely implemented technology used to address the access time to data stored in nonvolatile memory was flash memory. In that type of system, the read and write access was slow compared volatile memory. The Inventor conceived of the inventions claimed in the '184, '219, '880, and '537 patents as a way to enhance the access to data stored to nonvolatile memory.

10. For example, the Inventor developed a nonvolatile memory system to decrease the amount of time it takes to access information from the nonvolatile memory.

Advantage Over the Prior Art

11. The embodiments described by the '184, '219, '880, and '537 patents provide many advantages over the prior art, and in particular improve the operations of accessing data stored within a nonvolatile memory system. (*See* '219 patent at Abstract and '219 patent at Figure 1.) One advantage of the patented invention is decreasing retrieval time of data stored within a nonvolatile memory system. (*See* '184 patent at 4:37-43.)

12. Another advantage is enhanced read and write performance of the memory system. (*See* '880 patent at Abstract.)

13. Another advantage is enhancing the random access performance of nonvolatile IC, subsystem and system. (*See* '537 patent at 2:4-5.)

14. Yet another advantage is decreased latency. (*See* '219 patent at 4:46-49.)

15. Because of these significant advantages that can be achieved through the use of the embodiments of the '184, '219, '880, and '537 patents, Flash-Control believes that the '184, '219, '880, and '537 patents presents significant commercial value for companies like Micron. Indeed, Micron's NVDIMM technology, 3D XPoint memory technology, and SSDs are widely used to provide access to data stored within a nonvolatile memory system.

Technological Innovation

16. The embodiments disclosed in the '184, '219, '880, and '537 patents resolve technical problems related to nonvolatile memory storage systems, particularly problems related to the utilization of memory stored in nonvolatile memory storage. As the '184, '219, '880, and '537 patents explain, one of the limitations of the prior art regarding nonvolatile memory storage systems was that the performance time including the read time, program/write time is slow compared to volatile memory built with SRAMs and DRAMs. (*See* '219 patent at 1:56-58.)

17. The claims of the '184, '219, '880, and '537 patents do not merely recite the performance of some well-known business practice from the pre-Internet world along with the requirement to perform it on the Internet. Instead, the claims of the '184, '219, '880, and '537 patents recite inventive concepts that are deeply rooted in engineering technology, and are directed to problems specifically arising out of how to decrease the amount of time required to retrieve data stored in nonvolatile memory.

18. In addition, the claims of the ‘184, ‘219, ‘880, and ‘537 patents are directed to inventive concepts that improve the functioning of a nonvolatile memory system, particularly improving accessibility of stored data.

19. Moreover, the claims of the ‘184, ‘219, ‘880, and ‘537 patents are directed to inventive concepts that are not merely routine or conventional use of nonvolatile memory. Instead, the patented invention of the ‘184, ‘219, ‘880, and ‘537 patents is directed to a new and novel solution to specific problems related to nonvolatile memory systems.

20. And finally, the claimed invention of the ‘184, ‘219, ‘880, and ‘537 patents do not preempt nonvolatile memory systems, nor does the ‘184, ‘219, ‘880, and ‘537 patents preempt any other well-known or prior art technology.

21. Accordingly, the claims in the ‘184, ‘219, ‘880, and ‘537 patents recite a combination of elements sufficient to ensure that the claims in substance and in practice amount to significantly more than a patent-ineligible abstract idea.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 9,357,184

22. The allegations set forth in the foregoing paragraphs 1 through 21 are incorporated into this First Claim for Relief – Count 1.

23. On February 9,2016, the ’184 patent was duly and legally issued by the United States Patent and Trademark Office under the title “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES”

24. Flash-Control is the assignee and owner of the right, title and interest in and to the ’184 patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

25. Upon information and belief, Micron has and continues to directly infringe one or more claims of the '184 patent by selling, offering to sell, making, using (including without limitation testing), importing and/or providing and causing to be used products, specifically one or more of DDR4 SDRAM, NVRDIMM, NVDIMM products, products utilizing 3D XPoint memory, and solid-state drive that incorporates a memory controller and flash memory, which by way of example include https://www.micron.com/products/dram-modules/nvdimm, https://www.micron.com/products/advanced-solutions/3d-xpoint-technology and https://www.micron.com/products/solid-state-drives (the "Accused Instrumentalities").

26. Upon information and belief, the Accused Instrumentalities performs a method for decreasing the amount of time required to access data stored in the nonvolatile memory.

27. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory system such as a Micron NVDIMM technology including a nonvolatile memory. *See* Claim Chart for the '184 Patent, attached hereto as Exhibit E.

28. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage of digital information in addressable locations arranged in multiple blocks for access. Including, nonvolatile memory with protectable blocks with 128 bytes available for use by the end user. *Id.*

29. Upon information and belief, one or more of the Accused Instrumentalities includes requiring writing of modified digital information into a new physical location mapped to the same associated addressable location when reading any portion of the digital information in a given block from an associated addressable location and modification thereof for storage back in the memory in the same addressable location. Including, NVDIMMs with multiple devices connected to the system I^2C-compatible SMBus with system accessible address spaces

for these devices. Additionally, inherent to fly-by topology, the timing skew between the clock and the DQS signals can be accounted for by using the write-leveling feature of DDR4. Further, control words can be set by the host through the DRAM address and control bus or the I^2C bus interface. *Id.*

30. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory for read and write operations including a DRAM combined to a flash and intelligent system controller. Including, a DRAM combined to an intelligent system controller with single read or write access. *Id.*

31. Upon information and belief, one or more of the Accused Instrumentalities include a volatile random access memory coupled to nonvolatile memory for storage controlled by one or more controllers including combing DRAM and flash with an intelligent system controller. *Id*.

32. Upon information and belief, one or more of the Accused Instrumentalities includes one or more controllers to control volatile and nonvolatile memories to perform a read operation on the portion of the digital information to be read and retrieving and storing from the given block of memory at the associated addressable location. This includes devices that combine DRAM, flash, and an intelligent system controller and that have address inputs that provide the row address for active commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. *Id.*

33. Upon information and belief, one or more of the Accused Instrumentalities include accessing any portion of the stored retrieved digital information from the volatile random access memory. Including an NVDIMM that has protectable blocks with a fly-by topology.

And DDR4 SDRAM modules that use two sets of signals to capture data and commands, and an address. *Id*

34. Upon information and belief, one or more of the Accused Instrumentalities includes performing a read operation from the volatile memory of any portion or all of the stored digital information in the volatile memory. This includes devices that perform a single read for the DDR4 SDRAM module that effectively consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal DRAM core. *Id.*

35. Upon information and belief, one or more of the Accused Instrumentalities includes performing a write operation on any portion of the accessed read digital information from the volatile memory back to the same physical location in the volatile memory for storage therein. Including a device that performs a single write access for the DDR4 SDRAM module that effectively consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal DRAM core. *Id.*

36. Upon information and belief, one or more of the Accused Instrumentalities includes writing the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read. For example, the NVDIMM takes control of the SDRAM, and the SDRAM contents are backed up to the Flash memory. *Id.*

37. One or more of the Accused Instrumentalities infringed and continues to infringe claim 1 of the ’184 patent during the pendency of the ’184 patent.

38. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory system coupled to a central processing unit, including for example a host coupled to the NVDIMM. *Id.*

39. The Accused Instrumentality infringed and continues to infringe claim 2 of the '184 patent during the pendency of the '184 patent.

40. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage is a phase change memory. Including a phase change memory for mobile devices. *See* https://investors.micron.com/news-releases/news-release-details/micron-announces-availability-phase-change-memory-mobile-devices.

41. One or more of the Accused Instrumentality infringed and continues to infringe claim 4 of the '184 patent during the pendency of the '184 patent.

42. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage with a magnetic memory.

43. One or more of the Accused Instrumentality infringed and continues to infringe claim 5 of the '184 patent during the pendency of the '184 patent.

44. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage with a ferroelectric memory.

45. One or more of the Accused Instrumentality infringed and continues to infringe claim 6 of the '184 patent during the pendency of the '184 patent.

46. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage with a molecular memory.

47. One or more of the Accused Instrumentality infringed and continues to infringe claim 7 of the '184 patent during the pendency of the '184 patent.

48. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory with a SRAM with at least one port for read and write access.

49. One or more of the Accused Instrumentality infringed and continues to infringe claim 8 of the ‘184 patent during the pendency of the ‘184 patent.

50. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory that is a dynamic random access memory with at least one port for read and write access.

51. One or more of the Accused Instrumentality infringed and continues to infringe claim 9 of the ‘184 patent during the pendency of the ‘184 patent.

52. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory that is a pseudo static RAM with at least one port for read and write access.

53. One or more of the Accused Instrumentality infringed and continues to infringe claim 10 of the ‘184 patent during the pendency of the ‘184 patent.

54. Upon information and belief, one or more of the Accused Instrumentalities includes each block of the nonvolatile memory for storage having one or more pages of storegd data accessible through the coupled volatile random access memory.

55. One or more of the Accused Instrumentality infringed and continues to infringe claim 11 of the ‘184 patent during the pendency of the ‘184 patent.

56. Upon information and belief, one or more of the Accused Instrumentalities includes pages that are randomly addressable and accessible.

57. One or more of the Accused Instrumentality infringed and continues to infringe claim 12 of the ‘184 patent during the pendency of the ‘184 patent.

58. Upon information and belief, one or more of the Accused Instrumentalities includes pages that are serially addressable and accessible.

59. One or more of the Accused Instrumentality infringed and continues to infringe claim 13 of the '184 patent during the pendency of the '184 patent.

60. Upon information and belief, one or more of the Accused Instrumentalities includes pages that are randomly and serially addressable and accessible.

61. One or more of the Accused Instrumentality infringed and continues to infringe claim 14 of the '184 patent during the pendency of the '184 patent.

62. Upon information and belief, one or more of the Accused Instrumentalities includes each page of the block being able to be substituted on the fly for any other page of a different block through address mapping.

63. One or more of the Accused Instrumentality infringed and continues to infringe claim 15 of the '184 patent during the pendency of the '184 patent.

64. Upon information and belief, one or more of the Accused Instrumentalities includes each of the randomly addressable and accessible pages being capable of addressing at least one bit in each access.

65. One or more of the Accused Instrumentality infringed and continues to infringe claim 16 of the '184 patent during the pendency of the '184 patent.

66. On information and belief, the above identified infringement has been and continues to be willful.

67. Flash-Control has been harmed by the above identified infringing activities.

COUNT 2 – INFRINGEMENT OF U.S. PATENT NO. 9,792,219

68. The allegations set forth in the foregoing paragraphs 1 through 21 are incorporated into this First Claim for Relief.- Count 2.

69. On October 17, 2017, the ’219 patent was duly and legally issued by the United States Patent and Trademark Office under the title “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE.”

70. Flash-Control is the assignee and owner of the right, title and interest in and to the ’219 patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

71. Upon information and belief, Micron has infringed and continues to directly infringe one or more claims of the ’219 patent by selling, offering to sell, making, using (including without limitation testing), importing, and/or providing and causing to be used products, specifically one or more of DDR4 SDRAM, NVRDIMM, NVDIMM products, products utilizing 3D XPoint memory, and solid-state drive that incorporates a memory controller and flash memory, which by way of example include https://www.micron.com/products/dram-modules/nvdimm, https://www.micron.com/products/advanced-solutions/3d-xpoint-technology and https://www.micron.com/products/solid-state-drives (the “Accused Instrumentalities”).

72. Upon information and belief, the Accused Instrumentalities performs a method for decreasing the amount of time to access data stored in the nonvolatile memory.

73. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory system such as the Micron NVDIMM, which includes a nonvolatile memory. *See* Claim Chart for the ‘219 Patent, attached hereto as Exhibit F.

74. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory for storage of digital information arranged in multiple blocks for access, including, nonvolatile memory for storage with protectable blocks. *Id.*

75. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory for read and write operations coupled to said nonvolatile memory, including combing DRAM and flash, with single read or write access. *Id.*

76. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile random access memory and nonvolatile memory that are controlled by one or more controllers, including combing DRAM and flash with an intelligent system controller. *Id.*

77. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory system coupled to a central processing unit, including for example a host coupled to the NVDIMM. *Id.*

78. Upon information and belief, one or more of the Accused Instrumentalities includes a device having a nonvolatile memory in which each block of the nonvolatile memory for storage has one or more pages of stored data accessible through the coupled volatile random access memory, and each page of a block is adapted to be substituted on the fly for another page of a different block through addressing mapping. As an example, NVDIMM has protectable blocks with a fly-by topology. As another example, DDR4 SDRAM modules use two sets of signals to capture data and commands, and an address. *Id.*

79. Upon information and belief, one or more of the Accused Instrumentalities includes one or more controllers to control volatile and nonvolatile memories to perform a read operation on the portion of the digital information to be read and retrieving and storing from the given block of memory at the associated addressable location. Including devices that combine DRAM, flash, and an intelligent system controller and that have address inputs that provide the row address for active commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. *Id.*

80. Upon information and belief, one or more of the Accused Instrumentalities performs a read operation from the volatile memory of any portion or all of the stored digital information in the volatile memory. Including devices that perform a single read for the DDR4 SDRAM module that effectively consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal DRAM core. *Id.*

81. Upon information and belief, one or more of the Accused Instrumentalities preforms a write operation on any portion of digital information accessed from the volatile memory back to the same physical location in the volatile memory for storage therein. This includes a device that performs a single write access for the DDR4 SDRAM module that effectively consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal DRAM core. *Id.*

82. Upon information and belief, one or more of the Accused Instrumentalities writes the digital information stored in the volatile memory back to the nonvolatile memory at a different physical location with the same associated address from which it was read. For example, the NVDIMM takes control of the SDRAM, and the SDRAM contents are backed up to the Flash memory. *Id.*

83. One or more of the Accused Instrumentalities infringed and continue to infringe at least claim 1 of the ’219 patent during the pendency of the ’219 patent.

84. On information and belief, the above identified infringement has been and continues to be willful.

85. Flash-Control has been harmed by the above identified infringing activities.

COUNT III – INFRINGEMENT OF U.S. PATENT NO. 8,531,880

86. The allegations set forth in the foregoing paragraphs 1 through 21 are incorporated into this First Claim for Relief – Count 3.

87. On September 10, 2013, the ’880 patent was duly and legally issued by the United States Patent and Trademark Office under the title “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES”

88. Flash-Control is the assignee and owner of the right, title and interest in and to the ’880 patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

89. Upon information and belief, Micron has and continues to directly infringe one or more claims of the ’880 patent by selling, offering to sell, making, using (including without limitation testing), importing, and/or providing and causing to be used products, specifically one or more, of DDR4 SDRAM, NVRDIMM, NVDIMM products, products utilizing 3D XPoint memory, and solid-state drive that incorporates a memory controller and flash memory, which by way of example include https://www.micron.com/products/dram-modules/nvdimm, https://www.micron.com/products/advanced-solutions/3d-xpoint-technology and https://www.micron.com/products/solid-state-drives (the “Accused Instrumentalities”).

90. Upon information and belief, the Accused Instrumentalities performs a method for decreasing the amount of time required to access data stored in the nonvolatile memory.

91. Upon information and belief, one or more of the Accused Instrumentalities includes a memory system including a NAND combined to an SSD controller and DRAM buffer. *See* Claim Chart for the ‘880 Patent, attached as Exhibit G.

92. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory organized to include a plurality of blocks each having a plurality of pages. Including, a drive interface with a plurality of blocks having a plurality of pages. *Id.*

93. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory including a DRAM buffer. *Id.*

94. Upon information and belief, one or more of the Accused Instrumentalities includes a first buffer capable of temporarily storing at least one page including a buffer with 2,112 bytes. *Id.*

95. Upon information and belief, one or more of the Accused Instrumentalities includes a second buffer configured to receive information associated with one or more write requests, the write request being associated with one or more changes to one or more portions of a page in the non-volatile memory, the one or more portions being less than the entirety of the page. Including, a Buffer A and a Buffer B in communication with a control logic, registers, and a NAND Device. Further including, a data path with data and metadata where the data is written from the NAND media. *Id.*

96. Upon information and belief, one or more of the Accused Instrumentalities includes a system adapted to locate a page associated with one or more write requests in the nonvolatile memory, and to selectively write the page to the first buffer. Including, a system adapted to perform a copyback function. *Id.*

97. Upon information and belief, one or more of the Accused Instrumentalities includes a system adapted to locate in the first buffer one or more portions of the page associated with the one or more write requests, and to selectively write one or more portions to the volatile

memory without writing the entirety of the page in the first buffer to the volatile memory. Including, a system adapted to perform a copyback function or copyback program. *Id.*

98. Upon information and belief, one or more of the Accused Instrumentalities includes a system adapted to write said one or more changes from the second buffer to the volatile memory, thereby updating said one or more updated portions from the volatile memory to the first buffer. Including, a system including a Buffer A, a Buffer B, a Control Logic, a SRAM and a NAND Device. *Id.*

99. Upon information and belief, one or more of the Accused Instrumentalities includes updating the page stored in the first buffer to include one or more changes associated with the write requests. Including, a system adapted to perform a copyback function. *Id.*

100. Upon information and belief, one or more of the Accused Instrumentalities includes a system adapted to write the updated page from the first buffer to an erased page in the nonvolatile memory. Including a system adapted to perform a copyback function. *Id.*

101. One or more of the Accused Instrumentalities infringed and continues to infringe claim 1 of the ’880 patent during the pendency of the ’880 patent.

102. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory comprises a NAND flash memory including an SSD with NAND flash memory. *Id.*

103. One or more of Accused Instrumentalities infringed and continues to infringe claim 2 of the ‘880 patent during the pendency of the ‘880 patent.

104. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory that comprises a dynamic random access memory (DRAM) including an SSD with a DRAM buffer. *Id.*

105. One or more of Accused Instrumentalities infringed and continues to infringe claim 3 of the '880 patent during the pendency of the '880 patent.

106. Upon information and belief, one or more of the Accused Instrumentalities comprises a flash memory system including a controller coupled to a NAND and DRAM buffer. *Id.*

107. Upon information and belief, one or more of the Accused Instrumentalities includes a NAND flash memory organized to include a plurality of blocks each having a plurality of pages. Including an SSD with NAND and a plurality of blocks comprised of a plurality of pages. *Id.*

108. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory including a DRAM buffer. *Id.*

109. Upon information and belief, one or more of the Accused Instrumentalities includes a controller including an SSD controller. *Id.*

110. Upon information and belief, one or more of the Accused Instrumentalities includes a first buffer capable of temporarily storing at least one page including a buffer with 2,112 bytes. *Id.*

111. Upon information and belief, one or more of the Accused Instrumentalities includes a second buffer configured to receive information associated with one or more write requests, and write request being associated with one or more changes to one or more portions of a page in said NAND flash memory, the one or more portions being less than the entirety of the page. Including, a Buffer B in communication with a control logic, registers, and a NAND Device. Further including, a data path with data and metadata where the data is written from the NAND media. *Id.*

112. Upon information and belief, one or more of the Accused Instrumentalities includes the controller locating the page associated with the one or more write request in the NAND flash memory, and selectively writing the page from the NAND flash memory to the first buffer. Including a system adapted to perform a copyback definition. *Id.*

113. Upon information and belief, one or more of the Accused Instrumentalities includes the controller locating in said first buffer the one or more portions of the page associated with the one or more write requests, and selectively writing the page from the NAND flash memory to the first buffer. Including a NAND device that is adapted to perform a copyback program. *Id.*

114. Upon information and belief, one or more of the Accused Instrumentalities includes the controller locating in the first buffer the one or more portions of the page associated with the one or more portions to said volatile memory without writing the entirety of the page in the first buffer to the volatile memory. Including a controller adapted to perform a copyback program. *Id.*

115. Upon information and belief, one or more of the Accused Instrumentalities includes the controller writing the one or more changes from said second buffer to said volatile memory, thereby updating the one or more portions associated with the one or more write requests to include the one or more changes; and the controller writing the one or more updated portions from the volatile memory to the first buffer. Including, a controller communicating with a Buffer A, a Buffer B, a Control Logic, a SRAM and a NAND Device. *Id.*

116. Upon information and belief, one or more of the Accused Instrumentalities includes updating the page stored in the first buffer to include one or more changes associated

with said one or more write requests. Including, a controller adapted to perform a copyback function. *Id.*

117. Upon information and belief, one or more of the Accused Instrumentalities includes the controller writing the updated page from the first buffer to an erased page in said NAND flash memory. Including, a controller of a NAND device adapted to perform a copyback function. *Id.*

118. One or more of the Accused Instrumentalities infringed and continues to infringe claim 4 of the '880 patent during the pendency of the '880 patent.

119. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory comprising a dynamic random access memory (DRAM) including a DRAM buffer. *Id.*

120. One or more of the Accused Instrumentalities infringed and continues to infringe claim 5 of the '880 patent during the pendency of the '880 patent.

121. Upon information and belief, one or more of the Accused Instrumentalities includes a memory system including an SSD controller coupled to a NAND and a DRAM buffer. *Id.*

122. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory organized to include a plurality of blocks each having a plurality of pages including an SSD with NAND and a plurality of blocks comprised of a plurality of pages. *Id.*

123. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory including a DRAM buffer. *Id.*

124. Upon information and belief, one or more of the Accused Instrumentalities includes a first buffer capable of temporarily storing at least one page including a buffer with 2,122 bytes. *Id.*

125. Upon information and belief, one or more of the Accused Instrumentalities includes a second buffer configured to receive information associated with the one or more write requests, the write requests being associated with one or more portions of a page in the non-volatile memory, the one or more portions being less than the entirety of the page. Including, a Buffer B in communication with a control logic, registers, and a NAND Device. Further including, a data path with data and metadata where the data is written from the NAND media. *Id.*

126. Upon information and belief, one or more of the Accused Instrumentalities includes the method for writing said one or more changes requested by the one or more write requests to one or more portions of a page in the nonvolatile memory, comprising of the steps of receiving in the second buffer information associated with one or more write requests. Including, a Buffer B in communication with a Buffer A, a Control Logic, NAND Device, and SRAM.

127. Upon information and belief, one or more of the Accused Instrumentalities includes locating in the nonvolatile memory the page associated with one or more write requests and selectively writing the located page to the first buffer. Including, a method adapted to perform a copyback program. *Id.*

128. Upon information and belief, one or more of the Accused Instrumentalities includes locating in the first buffer the one or more portions of the page associated with one or more write requests and selectively writing the one or more portions of the volatile memory

without writing the entirety of the page in the first buffer to the volatile memory. Including, a method adapted to perform a copyback program. *Id.*

129. Upon information and belief, one or more of the Accused Instrumentalities includes writing the one or more changes from the second buffer to the volatile memory, thereby updating the one or more portions associated with the one or more write requests to include the one or more changes and writing the one or more updated portions from the volatile memory to the first buffer. Including, a controller communicating with a Buffer A, a Buffer B, a Control Logic, a SRAM and a NAND Device. *Id.*

130. Upon information and belief, one or more of the Accused Instrumentalities includes updating the pages stored in the first buffer to include the one or more changes associated with said one or more write requests including a method adapted to perform a copyback program. *Id.*

131. Upon information and belief, one or more of the Accused Instrumentalities includes writing the updated page from the first buffer to an erased page in the nonvolatile memory including a method adapted to perform a copyback program. *Id.*

132. One or more of the Accused Instrumentalities infringed and continues to infringe claim 6 of the ’880 patent during the pendency of the ’880 patent.

133. Upon information and belief, one or more of the Accused Instrumentalities includes a NAND flash as the nonvolatile memory including a NAND coupled to an SSD controller and DRAM buffer. *Id.*

134. One or more of the Accused Instrumentalities infringed and continues to infringe claim 7 of the ’880 patent during the pendency of the ’880 patent.

135. Upon information and belief, one or more of the Accused Instrumentalities includes a dynamic random access memory (DRAM) as said volatile memory including a DRAM buffer. *Id.*

136. One or more of the Accused Instrumentalities infringed and continues to infringe claim 8 of the '880 patent during the pendency of the '880 patent.

137. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory that comprises a static random access memory (SRAM). *Id.*

138. One or more of the Accused Instrumentalities infringed and continues to infringe claim 14 of the '880 patent during the pendency of the '880 patent.

139. Upon information and belief, one or more of the Accused Instrumentalities includes a first buffer that comprises a static random access memory (SRAM). *Id.*

140. One or more of the Accused Instrumentalities infringed and continues to infringe claim 15 of the '880 patent during the pendency of the '880 patent.

141. Upon information and belief, one or more of the Accused Instrumentalities includes providing a static random access memory (SRAM) as the volatile memory. *Id.*

142. One or more of the Accused Instrumentalities infringed and continues to infringe claim 16 of the '880 patent during the pendency of the '880 patent.

143. Upon information and belief, one or more of the Accused Instrumentalities includes providing a static random access memory (SRAM) as a first buffer. *Id.*

144. One or more of the Accused Instrumentalities infringed and continues to infringe claim 17 of the '880 patent during the pendency of the '880 patent.

145. On information and belief, the above identified infringement has been and continues to be willful.

146. Flash-Control has been harmed by the above identified infringing activities.

COUNT IV – INFRINGEMENT OF U.S. PATENT NO. 8,817,537

147. The allegations set forth in the foregoing paragraphs 1 through 21 are incorporated into this First Claim for Relief – Count 4.

148. On August 26, 2014, the ’537 patent was duly and legally issued by the United States Patent and Trademark Office under the title “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES.”

149. Flash-Control is the assignee and owner of the right, title and interest in and to the ’537 patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

150. Upon information and belief, Micron has and continues to directly infringe one or more claims of the ’537 patent by selling, offering to sell, making, using (including without limitation testing), importing, and/or providing and causing to be used products, specifically one or more, of DDR4 SDRAM, NVRDIMM, NVDIMM products, products utilizing 3D XPoint memory, and solid-state drive that incorporates a memory controller and flash memory, which by way of example include https://www.micron.com/products/dram-modules/nvdimm, https://www.micron.com/products/advanced-solutions/3d-xpoint-technology and https://www.micron.com/products/solid-state-drives (the “Accused Instrumentalities”).

151. Upon information and belief, the Accused Instrumentalities performs a method for decreasing the amount of time required to access data stored in the nonvolatile memory.

152. Upon information and belief, the Accused Instrumentality includes a memory system including an SSD controller combined with a NAND and a DRAM buffer. *See* Claim Chart for the ‘537 patent, attached hereto as Exhibit H.

153. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory organized to include a plurality of blocks each having a plurality of pages. Including, a drive interface with a plurality of blocks having a plurality of pages. *Id.*

154. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory including a DRAM buffer. *Id.*

155. Upon information and belief, one or more of the Accused Instrumentalities includes a first buffer capable of temporarily storing at least one page including a Buffer A with 2,112 bytes. *Id.*

156. Upon information and belief, one or more of the Accused Instrumentalities includes a second buffer configured to receive information associated with one or more write requests, the write request being associated with one or more changes to one or more portions of a page in the non-volatile memory, said one or more portions being less than the entirety of the page. Including, a Buffer B in communication with a control logic, registers, and a NAND Device. Further including, a data path with data and metadata where the data is written from the NAND media. *Id.*

157. Upon information and belief, one or more of the Accused Instrumentalities includes a system adapted to locate a page associated with one or more write requests in the nonvolatile memory, and to selectively write the page to the first buffer. Including, a system adapted to perform a copyback function. *Id.*

158. Upon information and belief, one or more of the Accused Instrumentalities includes a system adapted to locate in the first buffer one or more portions of the page associated with the one or more write requests, and to selectively write one or more portions to the volatile

memory without writing the entirety of the page in the first buffer to the volatile memory. Including, a system adapted to perform a copyback function or copyback program. *Id.*

159. Upon information and belief, one or more of the Accused Instrumentalities includes a system adapted to write the one or more changes from the second buffer to the volatile memory, thereby updating the one or more portions associated with the one or more write requests to include the one or more changes and the system adapted to write the one or more updated portions from the volatile memory to said first buffer. Including, a system comprising a Buffer A, a Buffer B, a Control Logic, a SRAM and a NAND Device. *Id.*

160. Upon information and belief, one or more of the Accused Instrumentalities includes updating the page stored in the first buffer to include one or more changes associated with the write requests. Including, a system adapted to perform a copyback function. *Id.*

161. One or more of the Accused Instrumentalities infringed and continues to infringe claim 1 of the ’537 patent during the pendency of the ’537 patent.

162. Upon information and belief, one or more of the Accused Instrumentalities includes a non-volatile memory that includes a multi-level cell (MLC) NAND flash memory. *Id.*

163. One or more of the Accused Instrumentalities infringed and continues to infringe claim 2 of the ’537 patent during the pendency of the ’537 patent.

164. Upon information and belief, one or more of the Accused Instrumentalities, includes a non-volatile memory that includes a multi-level cell (MLC) NAND flash memory. *Id.*

165. One or more of the Accused Instrumentalities infringed and continues to infringe claim 3 of the ’537 patent during the pendency of the ’537 patent.

166. Upon information and belief, one or more of the Accused Instrumentalities, includes a volatile memory including one of (i) a dynamic random access memory (DRAM) and (ii) a static random access memory (SRAM). *Id.*

167. One or more of the Accused Instrumentalities infringed and continues to infringe claim 5 of the '537 patent during the pendency of the '537 patent.

168. Upon information and belief, one or more of the Accused Instrumentalities, includes a first buffer including a static random access memory (SRAM). *Id.*

169. One or more of the Accused Instrumentalities infringed and continues to infringe claim 6 of the '537 patent during the pendency of the '537 patent.

170. Upon information and belief, one or more of the Accused Instrumentalities, includes a flash memory system including an SSD controller combined with a NAND and DRAM buffer. *Id.*

171. One or more of the Accused Instrumentalities infringed and continues to infringe claim 6 of the '537 patent during the pendency of the '537 patent.

172. Upon information and belief, one or more of the Accused Instrumentalities comprises a flash memory system including a controller coupled to a NAND and DRAM buffer. *Id.*

173. Upon information and belief, one or more of the Accused Instrumentalities includes a NAND flash memory organized to include a plurality of blocks each having a plurality of pages. Including an SSD with NAND and a plurality of blocks comprised of a plurality of pages. *Id.*

174. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory including a DRAM buffer. *Id.*

175. Upon information and belief, one or more of the Accused Instrumentalities includes a controller including an SSD controller. *Id.*

176. Upon information and belief, one or more of the Accused Instrumentalities includes a first buffer capable of temporarily storing at least one page including a buffer with 2,112 bytes. *Id.*

177. Upon information and belief, one or more of the Accused Instrumentalities includes a second buffer configured to receive information associated with one or more write requests, and write request being associated with one or more changes to one or more portions of a page in said NAND flash memory, the one or more portions being less than the entirety of the page. Including, a Buffer B in communication with a control logic, registers, and a NAND Device. Further including, a data path with data and metadata where the data is written from the NAND media. *Id.*

178. Upon information and belief, one or more of the Accused Instrumentalities includes the controller locating the page associated with the one or more write request in said NAND flash memory, and selectively writing the page from the NAND flash memory to the first buffer. Including a system adapted to perform a copyback definition. *Id.*

179. Upon information and belief, one or more of the Accused Instrumentalities includes the controller locating in the first buffer the one or more portions of the page associated with the one or more write requests, and selectively writing the page from the NAND flash memory to the first buffer. Including a NAND device that is adapted to perform a copyback program. *Id.*

180. Upon information and belief, one or more of the Accused Instrumentalities includes the controller locating in the first buffer the one or more portions of the page associated

with the one or more portions to said volatile memory without writing the entirety of the page in the first buffer to the volatile memory. Including a controller adapted to perform a copyback program. *Id.*

181. Upon information and belief, one or more of the Accused Instrumentalities includes the controller writing the one or more changes from the second buffer to the volatile memory, thereby updating the one or more portions associated with the one or more write requests to include the one or more changes; and the controller writing the one or more updated portions from the volatile memory to the first buffer. Including, a controller communicating with a Buffer A, a Buffer B, a Control Logic, a SRAM and a NAND Device. *Id.*

182. Upon information and belief, one or more of the Accused Instrumentalities includes updating the page stored in the first buffer to include one or more changes associated with the one or more write requests. Including, a controller adapted to perform a copyback function. *Id.*

183. One or more of the Accused Instrumentalities infringed and continues to infringe claim 7 of the ’537 patent during the pendency of the ’537 patent.

184. Upon information and belief, one or more of the Accused Instrumentalities includes a NAND flash memory that includes a multi-level cell (MLC) NAND flash memory. *Id.*

185. One or more of the Accused Instrumentalities infringed and continues to infringe claim 8 of the ’537 patent during the pendency of the ’537 patent.

186. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory that includes one of (i) a dynamic random access memory (DRAM) and (ii) a static random access memory (SRAM).

187. One or more of the Accused Instrumentalities infringed and continues to infringe claim 10 of the ’537 patent during the pendency of the ’537 patent.

188. Upon information and belief, one or more of the Accused Instrumentalities includes a memory system including an SSD controller coupled to a NAND and a DRAM buffer. *Id.*

189. Upon information and belief, one or more of the Accused Instrumentalities includes a nonvolatile memory organized to include a plurality of blocks each having a plurality of pages including an SSD with NAND and a plurality of blocks comprised of a plurality of pages. *Id.*

190. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory including a DRAM buffer. *Id.*

191. Upon information and belief, one or more of the Accused Instrumentalities includes a first buffer capable of temporarily storing at least one page including a Buffer A with 2,122 bytes. *Id.*

192. Upon information and belief, one or more of the Accused Instrumentalities includes a second buffer configured to receive information associated with the one or more write requests, the write requests being associated with one or more portions of a page in said non-volatile memory, the one or more portions being less than the entirety of the page. Including, a Buffer B in communication with a control logic, registers, and a NAND Device. Further including, a data path with data and metadata where the data is written from the NAND media. *Id.*

193. Upon information and belief, one or more of the Accused Instrumentalities includes the method for writing said one or more changes requested by said one or more write

requests to one or more portions of a page in said nonvolatile memory, comprising of the steps of receiving in the second buffer information associated with one or more write requests. Including, a Buffer B in communication with a Buffer A, a Control Logic, NAND Device, and SRAM.

194. Upon information and belief, one or more of the Accused Instrumentalities includes locating in the nonvolatile memory the page associated with one or more write requests and selectively writing the located page to the first buffer. Including, a method adapted to perform a copyback program. *Id.*

195. Upon information and belief, one or more of the Accused Instrumentalities includes locating in the first buffer the one or more portions of the page associated with one or more write requests and selectively writing the one or more portions of the volatile memory without writing the entirety of the page in the first buffer to the volatile memory. Including, a method adapted to perform a copyback program. *Id.*

196. Upon information and belief, one or more of the Accused Instrumentalities includes writing the one or more changes from the second buffer to the volatile memory, thereby updating the one or more portions associated with the one or more write requests to include the one or more changes and writing the one or more updated portions from the volatile memory to the first buffer. Including, a controller communicating with a Buffer A, a Buffer B, a Control Logic, a SRAM and a NAND Device. *Id.*

197. Upon information and belief, one or more of the Accused Instrumentalities includes updating the pages stored in the first buffer to include the one or more changes associated with said one or more write requests including a method adapted to perform a copyback program. *Id.*

198. One or more of the Accused Instrumentalities infringed and continues to infringe claim 12 of the ’537 patent during the pendency of the ’537 patent.

199. Upon information and belief, one or more of the Accused Instrumentalities includes providing a multi-level cell (MLC) NAND flash memory as said non-volatile memory. *Id.*

200. One or more of the Accused Instrumentalities infringed and continues to infringe claim 13 of the ’537 patent during the pendency of the ’537 patent.

201. Upon information and belief, one or more of the Accused Instrumentalities includes providing a NAND flash memory as said non-volatile memory including a NAND combined to an SSD and a DRAM buffer. *Id.*

202. One or more of the Accused Instrumentalities infringed and continues to infringe claim 14 of the ’537 patent during the pendency of the ’537 patent

203. Upon information and belief, one or more of the Accused Instrumentalities includes a volatile memory one of (i) a dynamic random access memory (DRAM) and (ii) a static random access memory (SRAM). *Id.*

204. One or more of the Accused Instrumentalities infringed and continues to infringe claim 15 of the ’537 patent during the pendency of the ’537 patent.

205. Upon information and belief, one or more of the Accused Instrumentalities includes a static random access memory (SRAM) as said first buffer. *Id.*

206. One or more of the Accused Instrumentalities infringed and continues to infringe claim 16 of the ’537 patent during the pendency of the ’537 patent.

207. On information and belief, the above identified infringement has been and continues to be willful.

208. Flash-Control has been harmed by the above identified infringing activities.

JURY DEMAND

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Flash-Control demands a trial by jury on all issues triable as such.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Flash-Control demands judgment for itself and against Micron as follows:

A. An adjudication that Micron has infringed the '184, '219, '880, and '537 patents;

B. An award of damages to be paid by Micron adequate to compensate Flash-Control for Micron's past infringement of the '184, '219, '880, and '537 patents, and any continuing or future infringement through the date such judgment is entered, including interest, costs, expenses and an accounting of all infringing acts including, but not limited to, those acts not presented at trial;

C. A declaration that this case is exceptional under 35 U.S.C. § 285, and an award of Flash-Control's reasonable attorneys' fees; and

D. An award to Flash-Control of such further relief at law or in equity as the Court deems just and proper.

Dated: May 4, 2020

DEVLIN LAW FIRM LLC

/s/ Alex Chan

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